FAST PARALLEL CALCULATION OF CYCLIC REDUNDANCY CHECKS

ABSTRACT

Circuits, methods, and apparatus for the fast parallel calculation of CRCs. One embodiment provides a feedforward path that combines common terms to simplify input logic. Common expressions that appear in multiple terms in the feedforward path are implemented using logic gates that are shared by the multiple terms, thereby reducing logic complexity, fan-out, and gate delay. Another embodiment provides a CRC logic architecture having a feedback path that is able to use more than one clock cycle in its computation.